

## 28F002BC 2-MBIT (256K X 8) BOOT BLOCK FLASH MEMORY

- **High Performance Read**
  - 80/120 ns Max Access Time
  - 40 ns Max. Output Enable Time
- **Low Power Consumption**
  - 20 mA Typical Read Current
- **x8-Only Input/Output Architecture**
  - Space-Constrained 8-bit Applications
- **Optimized Array Blocking Architecture**
  - One 16-KB Protected Boot Block
  - Two 8-KB Parameter Blocks
  - One 96-KB Main Block
  - One 128-KB Main Block
  - Top Boot Location
- **Hardware Data Protection Feature**
  - Erase/Write Lockout during Power Transitions
  - Absolute Hardware Protection for Boot Block
- **Software EEPROM Emulation with Parameter Blocks**
- **Extended Cycling Capability**
  - 100,000 Block Erase Cycles
- **Automated Byte Write and Block Erase**
- **Industry-Standard Command User Interface**
  - Status Registers
  - Erase Suspend Capability
- **SRAM-Compatible Write Interface**
- **Reset/Deep Power-Down Input**
  - 0.2  $\mu$ A  $I_{CC}$  Typical
  - Provides Reset for Boot Operations
- **Industry-Standard Surface Mount Packaging**
  - 40-Lead TSOP
  - 44-Lead PSOP
- **ETOX™ IV Flash Technology**
  - 5V Read
- **12V Write and Block Erase**
  - $V_{PP} = 12V \pm 5\%$  Standard
  - $V_{PP} = 12V \pm 10\%$  Option
- **Independent Software Vendor Support**

Intel's 2-Mbit flash memory is an extension of the Boot Block architecture which includes block-selective erasure, automated write and erase operations, and a standard microprocessor interface. The 2-Mbit flash memory enhances the Boot Block architecture by adding more density and blocks, x8 input/output control, very high-speed, low-power, and industry-standard ROM-compatible pinout and surface mount packaging.

The Intel 28F002BC is an 8-bit wide flash memory offering. This high-density flash memory provides user-selectable bus operation for 8-bit applications. The 28F002BC is a 2,097,152-bit nonvolatile memory organized as 262,144 bytes of information. It is offered in 44-lead PSOP and 40-lead TSOP packages, which are ideal for space-constrained portable systems or any application with board space limitations.

This device uses an integrated Command User Interface (CUI) and Write State Machine (WSM) for simplified byte write and block erasure. The 28F002BC provides block locations compatible with Intel's MCS®-186 family, 80286, 90860CA, and the Intel386™, Intel486™, Pentium®, and Pentium Pro microprocessors.

The boot block includes a data protection feature to protect the boot code in critical applications. With a maximum access time of 80 ns, this high-performance 2-Mbit flash memory interfaces at zero wait-state to a wide range of microprocessors and microcontrollers. A deep power-down mode lowers the total  $V_{CC}$  power consumption to 1  $\mu$ W typical. This power savings is critical in hand-held battery powered systems. For very low-power applications using a 3.3V supply, refer to the Intel 28F002BV-T/B *2-Mbit SmartVoltage Boot Block Flash Memory* datasheet. Manufactured on Intel's 0.6 micron ETOX™ IV process technology, the 28F002BC flash memory provides world-class quality, reliability, and cost-effectiveness at the 2-Mbit density.

Information in this document is provided in connection with Intel products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

\*Third-party brands and names are the property of their respective owners.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation  
P.O. Box 7641  
Mt. Prospect, IL 60056-7641

or call 1-800-879-4683

COPYRIGHT © INTEL CORPORATION, 1996

CG-041493

# CONTENTS

	PAGE		PAGE
<b>1.0 INTRODUCTION.....</b>	<b>5</b>	3.4 Boot Block Locking .....	22
1.1 Designing for Density Upgradeability .....	5	3.4.1 VPP = V <sub>IL</sub> for Complete Protection .....	22
1.2 Main Features.....	5	3.4.2 RP# = V <sub>HH</sub> for Boot Block Unlocking....	22
1.3 Applications .....	6	3.5 Power Consumption.....	22
1.4 Pinouts .....	7	3.5.1 Active Power .....	22
1.5 Pin Descriptions.....	9	3.5.2 Standby Power.....	22
		3.5.3 Deep Power-Down .....	22
<b>2.0 PRODUCT DESCRIPTION .....</b>	<b>10</b>	3.6 Power-Up/Down Operation .....	22
2.1 Memory Organization .....	11	3.6.1 RP# Connected to System Reset.....	23
2.1.1 Blocking .....	11	3.6.2 V <sub>CC</sub> , V <sub>PP</sub> and RP# Transitions.....	23
2.1.2 28F002BC-T Block Memory Map .....	11	3.7 Power Supply Decoupling .....	23
		3.7.1 V <sub>PP</sub> Trace on Printed Circuit Boards....	23
<b>3.0 PRINCIPLES OF OPERATION.....</b>	<b>11</b>	<b>4.0 ELECTRICAL SPECIFICATIONS .....</b>	<b>24</b>
3.1 Bus Operations.....	12	4.1 Absolute Maximum Ratings .....	24
3.2 Read Operations.....	12	4.2 Operating Conditions .....	24
3.2.1 Read Array.....	12	4.2.1 Capacitance .....	25
3.2.2 Intelligent Identifiers .....	13	4.2.2 Input/Output Test Conditions.....	25
3.3 Write Operations.....	13	4.2.3 DC Characteristics .....	26
3.3.1 Command User Interface (CUI).....	13	4.2.4 AC Characteristics .....	28
3.3.2 Status Register .....	16	<b>APPENDIX A: Ordering Information .....</b>	<b>34</b>
3.3.3 Program Mode .....	17	<b>APPENDIX B: Additional Information.....</b>	<b>35</b>
3.3.4 Erase Mode .....	18		
3.3.5 Extended Cycling.....	18		



REVISION HISTORY

Number	Item
-001	Original version
-002	Pin 2 of 44-Lead PSOP changed from DU to NC

## 1.0 INTRODUCTION

This datasheet comprises the specifications for the 28F002BC 2-Mbit flash memory. Section 1 provides an overview of the 2-Mbit flash memory, including applications, pinouts, and pin descriptions. Section 2 describes the memory organization in detail. Section 3 defines a description of the memory's principles of operation. Finally, Section 4 details the memory's operating specifications.

### 1.1 Designing for Density Upgradeability

The 28F002BC has been optimized to meet market requirements. Applications currently using the 28F001BX and 28F002BX can migrate to this product. Of course, both the 28F001BX and the 28F002BX devices use an 8-bit wide bus. Those applications needing a 16-bit wide bus or lower voltage can convert to the SmartVoltage family of flash memory products.

SmartVoltage is also the natural migration path to the 4-Mbit density. Both the 28F002BC and the 4-Mbit SmartVoltage are offered in identical packages to make upgrade seamless. A few simple considerations can smooth the migration path significantly:

1. Connect the NC pin of the 28F002BC to GND (this will retain boot block locking when a 4-Mbit SmartVoltage is inserted).
2. Design a switchable  $V_{PP}$  to take advantage of the 5V  $V_{PP}$  option on SmartVoltage devices.
3. If anticipating to use the 5V  $V_{PP}$  option, switch  $V_{PP}$  to GND for complete write protection.

Previous designs with Intel's 28F002BX devices on occasion had to use a NOR gate (or some other scheme) to prevent issues with floating addresses latching incorrect data. The 28F002BC has corrected this issue and does not need the NOR gate. When migrating a design using the 28F002BX to the 28F002BC, the NOR gate can be removed. When considering upgrading, packaging is of paramount importance. Current and future market trends indicate TSOP and PSOP as the packages that will enable designs into the next century.

## 1.2 Main Features

The 28F002BC Boot Block flash memory is a high-performance, 2-Mbit (2,097,152 bit) flash memory organized as 256 Kbytes (262,144 bytes) of 8 bits each.

The 28F002BC has separately erasable blocks, including a hardware-lockable boot block (16,384 bytes), two parameter blocks (8,192 bytes each) and two main blocks (one block of 98,304 bytes and one block of 131,072 bytes). An erase operation typically erases one of the main blocks in 2.4 seconds and the boot or parameter blocks in 1.0 second. Each block can be independently erased and programmed 100,000 times.

The boot block is located at the top of the address map to match the protocol of many systems, including Intel's MCS-186 family, 80960CA, i860™ microprocessors as well as Pentium and Pentium Pro microprocessors. The hardware lockable boot block provides the most secure code storage. The boot block is intended to store the kernel code required for booting-up a system. When the RP# pin is between 11.4V and 12.6V, the boot block is unlocked and program and erase operations can be performed. When the RP# pin is at or below 6.5V, the boot block is locked and program and erase operations to the boot block are ignored.

The Command User Interface (CUI) serves as the interface between the microprocessor or microcontroller and the internal operation of the 28F002BC.

Program and Erase Automation allows program and erase operations to be executed using an industry standard two-write command sequence to the CUI. Data writes are performed in byte increments. Each byte in the flash memory can be programmed independently of other memory locations but is erased simultaneously with all other locations within the block.

The status register (SR) indicates the status of the internal Write State Machine (WSM), which reports critical information on program and/or erase sequences.

The maximum access time of 80 ns ( $t_{ACC}$ ) is guaranteed over the commercial temperature range (0°C to +70°C), 10%  $V_{CC}$  supply voltage range (4.5V to 5.5V) and 100 pF output load.

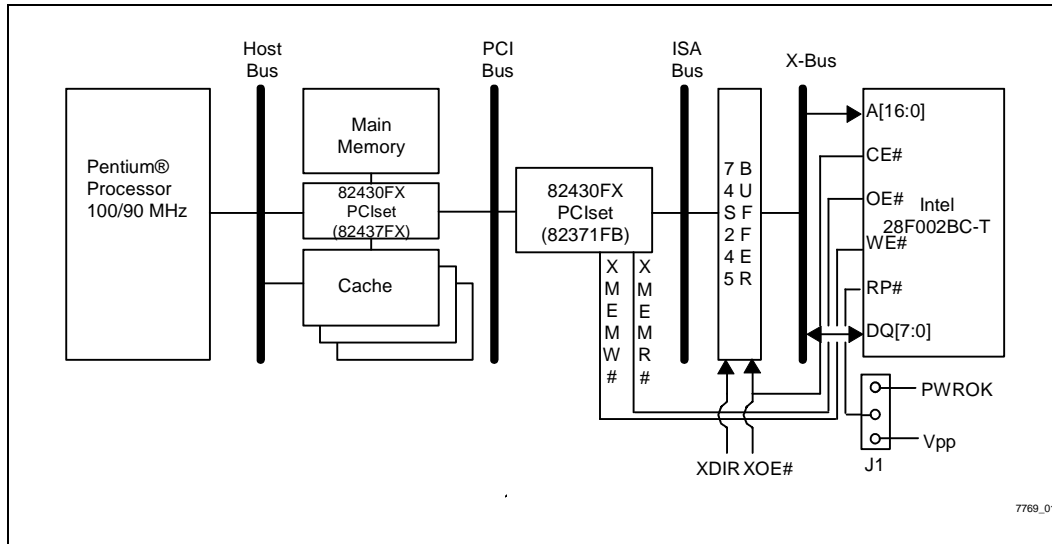


Figure 1. 28F002BC-T Interface to a Pentium® Microprocessor System

$I_{PP}$ , the maximum program current, is 20 mA. The  $V_{PP}$  voltage for erase and program is 11.4V to 12.6V ( $V_{PP} = 12V \pm 5\%$ ) under all operating conditions. Typical  $I_{CC}$  active current is 20 mA.

The 28F002BC flash memory is also designed with a standby mode to minimize system current drain and allow for low power designs. When the CE# and RP# pins are at  $V_{CC}$ , the CMOS standby mode is enabled and  $I_{CC}$  drops to about 50  $\mu A$ .

A deep power-down mode is enabled when the RP# pin is at ground. In addition to minimizing power consumption, the deep power-down mode also provides write protection during power-up conditions.  $I_{CC}$  current during deep power-down mode is 0.20  $\mu A$  typical. An initial maximum access time or reset time of 300 ns is required from RP# switching high until outputs are valid. Equivalently, the device has a maximum wake-up time of 215 ns until writes to the CUI are recognized.

When RP# is at ground, the WSM is reset, the status register is cleared, and the entire device is write-protected. This feature prevents data corruption and protects the code stored in the device during system reset. The system Reset pin can be tied to RP# to reset the memory to read mode at power-up. With on-chip program/erase

automation and RP# functionality for data protection, the device is protected against unwanted program and/or erase cycles, even during system reset.

### 1.3 Applications

2-Mbit Boot Block flash memory combines high density, high performance, and cost-effective flash memory with blocking and hardware protection capabilities. Its flexibility and versatility reduces cost throughout the product life cycle. Flash memory is ideal for Just-In-Time production flow, reducing system inventory and costs, and eliminating component handling during the production phase. During a product's life cycle, flash memory reduces costs by allowing user-performed code updates and feature enhancements via floppy disk or remote link.

The 28F002BC is a full-function blocked flash product suitable for a wide range of applications, including extended PC BIOS, digital cellular phone program and data storage, telecommunication boot/firmware, and various embedded applications where both program and data storage are required.

Reprogrammable systems, such as personal computers, are ideal applications for the 28F002BC. Portable and hand-held personal computer applications are becoming more complex with the addition of power management software to take advantage of the latest microprocessor technology, the availability of ROM-based application software, pen tablet code for electronic handwriting, and diagnostic code. Figure 1 shows an example 28F002BC-T application.

The increase in software sophistication augments the probability that a code update will be required after the PC is shipped. The 28F002BC provides a safe and inexpensive update solution for desktop, notebook, and hand-held personal computers while extending the product lifetime. Furthermore, the deep power-down mode provides added flexibility for those battery-operated portable designs that require low power.

The 28F002BC is also an excellent design solution for analog and digital cellular phone and telecommunication switching applications requiring high-performance, high-density storage in a small form factor package (x8-only bus). The blocking structure allows for easy segmentation of embedded code for modular software designs. For example, the parameter block can be used for frequently updated data storage and diagnostic messages (e.g., phone numbers and authorization codes).

1.4 Pinouts

The 28F002BC in the 44-lead PSOP pinout follows the industry standard ROM/EPROM pinout, as shown in Figure 3. The 2-Mbit SmartVoltage pinout, indicating the WP# input, is also shown in the same diagram. The 40-lead TSOP package (shown in Figure 2) offers the smallest form factor possible in addition to being compatible with its SmartVoltage upgrade in the same package.

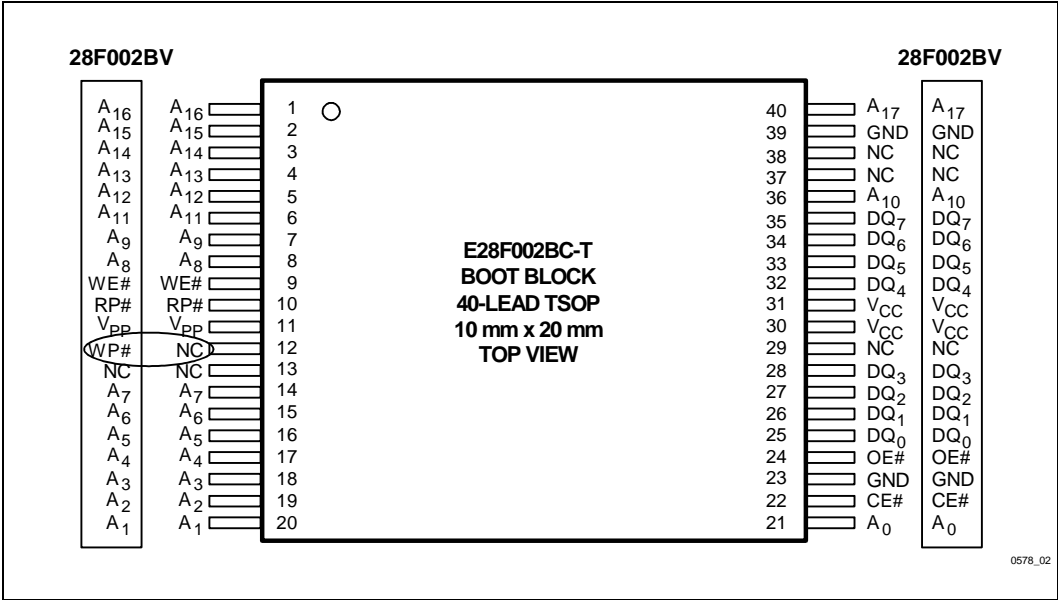


Figure 2. The 40-Lead TSOP Offers the Smallest Form Factor for Space-Constrained Applications

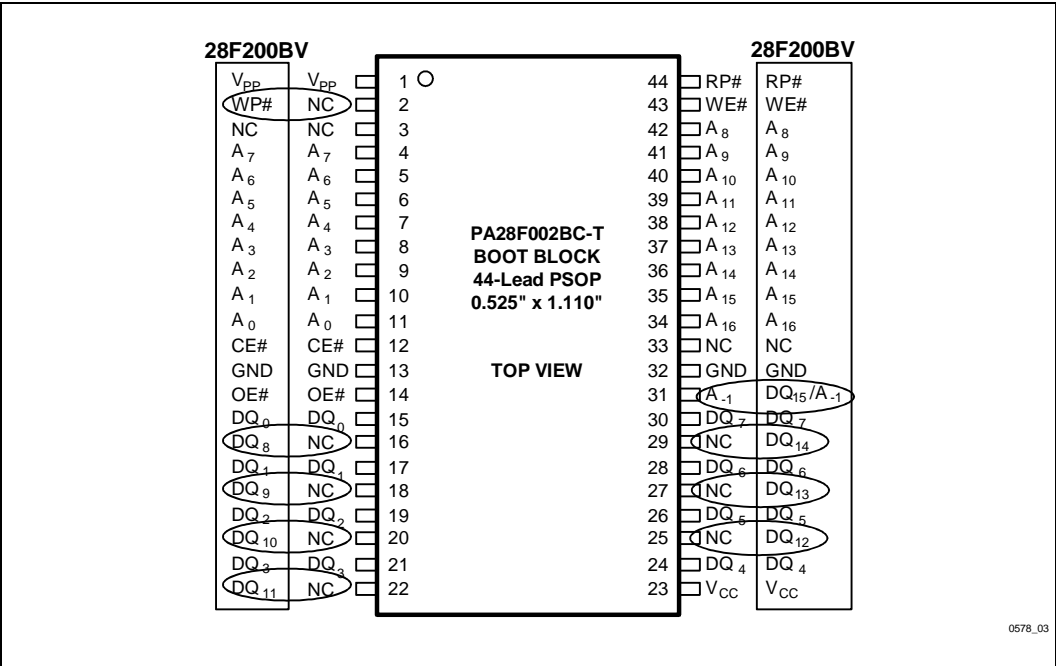


Figure 3. The 44-Lead PSOP Offers a Convenient Upgrade from JEDEC ROM Standards



## 1.5 Pin Descriptions

Table 1. 28F002BC Pin Descriptions

Symbol	Type	Name and Function
A <sub>-1</sub> , A <sub>0</sub> –A <sub>17</sub>	INPUT	<b>ADDRESS INPUTS</b> for memory addresses. Addresses are internally latched during a write cycle. A <sub>-1</sub> is used on the PSOP package only. A <sub>17</sub> is used only on the TSOP package
A <sub>9</sub>	INPUT	<b>ADDRESS INPUT:</b> When A <sub>9</sub> is at V <sub>HH</sub> , the signature mode is accessed. During this mode, A <sub>0</sub> decodes between the manufacturer and device IDs.
DQ <sub>0</sub> – .DQ <sub>7</sub>	INPUT/ OUTPUT	<b>DATA INPUTS/OUTPUTS:</b> Inputs array data on the second CE# and WE# cycle during a program operation. Inputs commands to the Command User Interface when CE# and WE# are active. Data is internally latched during the write cycle. Outputs array, Intelligent Identifier and Status register data. The data pins float to tri-state when the chip is de-selected or the outputs are disabled.
CE#	INPUT	<b>CHIP ENABLE:</b> Activates the device's control logic, input buffers, decoders and sense amplifiers. CE# is active low. CE# high deselected the memory device and reduces power consumption to standby levels. If CE# and RP# are high, but not at a CMOS high level, the standby current will increase due to current flow through the CE# and RP# input stages.
OE#	INPUT	<b>OUTPUT ENABLE:</b> Enables the device's outputs through the data buffers during a read cycle. OE# is active low.
WE#	INPUT	<b>WRITE ENABLE:</b> Controls writes to the Command Register and array blocks. WE# is active low. Addresses and data are latched on the rising edge of the WE# pulse.
RP#	INPUT	<b>RESET/DEEP POWER-DOWN:</b> Provides three-state control. Puts the device in deep power-down mode, locks, and unlocks the boot block from program/erase.  When RP# is at logic high level (6.5V maximum), the boot block is locked and cannot be programmed or erased.  When RP# = V <sub>HH</sub> (11.4V minimum), the boot block is unlocked and can be programmed or erased.  When RP# is at a logic low level the boot block is locked, the deep power-down mode is enabled and the WSM is reset preventing any blocks from being programmed or erased. When RP# transitions from logic low to logic high, the flash memory enters the read array mode.
V <sub>CC</sub>		<b>DEVICE POWER SUPPLY:</b> 5.0V ± 10%, 5.0V ± 5%
V <sub>PP</sub>		<b>PROGRAM/ERASE POWER SUPPLY:</b> For erasing memory array blocks or programming data in each block. When V <sub>PP</sub> < V <sub>PPLK</sub> all blocks are locked and memory contents cannot be altered.
GND		<b>GROUND:</b> For all internal circuitry.
NC		<b>NO CONNECT:</b> Pin may be driven or left floating.

The diagram illustrates the internal architecture of the M25P16 1-Mbit SPI Flash Memory. It shows the following components and their interconnections:

- Input/Output Buffers:** An **Input Buffer** at the top left receives data from the **Data Register** and the **Output Multiplexer**. An **Output Buffer** at the top right sends data to the **Data Register** and the **Output Multiplexer**. Both buffers are connected to the **DQ<sub>0</sub>-DQ<sub>7</sub>** data bus.
- Control and Status Registers:** The **Command User Interface** (receiving **CE#**, **WE#**, **OE#**, and **RP#**) is connected to the **Data Register**, **Status Register**, and **Identifier Register**. The **Status Register** is also connected to the **Output Multiplexer**.
- Data Path:** The **Data Register** is connected to the **Data Comparator** and the **Output Multiplexer**. The **Data Comparator** is also connected to the **Output Multiplexer**.
- Memory Array:** The **Y-Gating/Sensing** block contains five main sections: **16-Kbyte Boot Block**, **8-Kbyte Parameter Block**, **8-Kbyte Parameter Block**, **96-Kbyte Main Block**, and **128-Kbyte Main Block**. It is connected to the **Y-Decoder** and **X-Decoder**.
- Address Decoding:** The **Input Buffer** (bottom left) receives **A<sub>0</sub>-A<sub>17</sub>** and is connected to the **Address Latch** and **Address Counter**. The **Address Latch** is connected to the **Y-Decoder** and **X-Decoder**. The **Address Counter** is connected to the **Y-Decoder** and **X-Decoder**.
- Power and Voltage Control:** The **Power Reduction Control** block is connected to the **Y-Gating/Sensing** block and the **Write State Machine**. The **Write State Machine** is connected to the **Program/Erase Voltage Switch**, which is connected to **V<sub>PP</sub>**.
- I/O Logic:** The **I/O Logic** block is connected to the **Command User Interface** and the **Input Buffer**.

Power supply connections are indicated at the bottom right: **V<sub>CC</sub>** and **GND** for the main memory array, and **V<sub>PP</sub>** for the programming/erasing circuitry.

10

**PRELIMINARY**



## 2.1 Memory Organization

### 2.1.1 BLOCKING

The 28F002BC features an asymmetrically-blocked architecture that provides system memory integration. Each block can be erased up to 100,000 times. The block sizes have been chosen to optimize their functionality for common applications of nonvolatile storage. For the address locations of the blocks, see the memory map in Figure 5.

#### 2.1.1.1 Boot Block - 16 KB

The boot block is intended to replace a dedicated boot PROM in a microprocessor or microcontroller-based system. The 16-Kbyte (16,384 bytes) boot block is located at the top of the address map as shown in Figure 5. This boot block features hardware controllable write-protection to protect the crucial microprocessor boot code from accidental erasure. The boot block can be erased and written when RP# is held at 12V for the duration of the erase or program operation. This feature allows customers to change the boot code when necessary while providing security at other times.

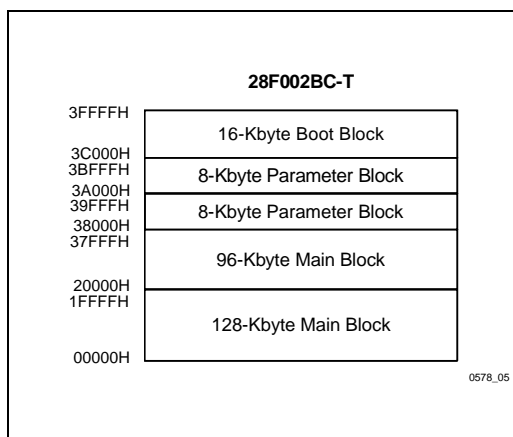


Figure 5. 28F002BC-T Memory Map

#### 2.1.1.2 Parameter Blocks - 8 KB (each)

The 28F002BC has two 8-Kbyte parameter blocks to facilitate storage of frequently updated system parameters that would normally require an EEPROM. The parameter blocks can also be used to store additional boot or main code. By using software techniques, the byte-rewrite functionality of EEPROMs can be emulated. These techniques are detailed in Intel's application note *AP-604 Using Intel's Boot Block Flash Memory Parameter Blocks to Replace EEPROM*.

#### 2.1.1.3 Main Block - 96 KB and 128 KB

The 28F002BC contains one 96-Kbyte (98,304 byte) block and one 128-Kbyte (131,072 byte) block. These blocks are typically used for data or code storage.

### 2.1.2 28F002BC-T BLOCK MEMORY MAP

The 16-Kbyte boot block of the 28F002BC-T is located from 3C000H to 3FFFFH. The first 8-Kbyte parameter block resides in memory space from 3A000H to 3BFFFH. The second 8-Kbyte parameter block consumes the memory area from 38000H to 39FFFH. The 96-Kbyte main block extends from 20000H to 37FFFH, while the 128-Kbyte main block occupies the region from 00000H to 1FFFFH.

## 3.0 PRINCIPLES OF OPERATION

Flash memory improves upon EPROM capability with in-circuit electrical write and erase. The Boot Block flash memory utilizes a Command User Interface (CUI) and automated algorithms to simplify write and erase operations. The CUI allows for 100% TTL-level control inputs, fixed power supplies during erasure and programming, and maximum EPROM compatibility.

When  $V_{PP} < V_{PPLK}$ , the device will only successfully execute the following commands: Read Array, Read Status register, Clear Status register, and Intelligent Identifier. The device provides standard EPROM read, standby and output disable operations. Manufacturer identification and device identification data can be accessed through the CUI or through the standard EPROM  $A_9$  high voltage ( $V_{ID}$ ) access for PROM programming equipment. High voltage on  $V_{PP}$  allows write and erase of the device. With  $V_{PP}$  active, all functions associated

with altering memory contents are accessible via the CUI.

The purpose of the Write State Machine (WSM) is to automate the write and erasure of the device completely. The WSM will begin operation upon receipt of a signal from the CUI and will report status back through the status register. The CUI will handle the WE# interface to the data and address latches, as well as system software requests for status while the WSM is in operation.

### 3.1 Bus Operations

Flash memory reads, erases and writes in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles. These bus operations are summarized in Tables 2 and 4.

### 3.2 Read Operations

The 28F002BC has three user read modes: read array, read intelligent identifier, and read status register

During power-up conditions, it takes a maximum of 600 ns from when  $V_{CC}$  is at 4.5V to when valid data is available at the outputs.

#### 3.2.1 READ ARRAY

When RP# transitions from  $V_{IL}$  (reset) to  $V_{IH}$ , the device will be in read array mode and will respond to the read control inputs (CE#, OE#, and address inputs) without any commands being written to the CUI.

When the device is in read array mode, four control signals must be manipulated to read data at the outputs.

- WE# must be logic high ( $V_{IH}$ )
- CE# must be logic low ( $V_{IL}$ )
- OE# must be logic low ( $V_{IL}$ )
- RP# must be logic high ( $V_{IH}$ )

In addition, the address of the desired location must be applied to the address pins. Refer to AC Characteristics for the exact sequence and timing of these signals.

If the device is not in read array mode, as would be the case after a program or erase operation, the Read Mode command (FFH) must be written to the CUI before reads can take place.

**Table 2. 28F002BC Bus Operations**

Mode	Notes	RP#	CE#	OE#	WE#	A <sub>9</sub>	A <sub>0</sub>	V <sub>PP</sub>	DQ <sub>0-7</sub>
Read	1,2,3	$V_{IH}$	$V_{IL}$	$V_{IL}$	$V_{IH}$	X	X	X	D <sub>OUT</sub>
Output Disable		$V_{IH}$	$V_{IL}$	$V_{IH}$	$V_{IH}$	X	X	X	High Z
Standby		$V_{IH}$	$V_{IH}$	X	X	X	X	X	High Z
Deep Power-Down	8	$V_{IL}$	X	X	X	X	X	X	High Z
Intelligent Identifier (Mfr)	4	$V_{IH}$	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{ID}$	$V_{IL}$	X	89H
Intelligent Identifier (Device)	4	$V_{IH}$	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{ID}$	$V_{IH}$	X	7CH
Write	5,6,7	$V_{IH}$	$V_{IL}$	$V_{IH}$	$V_{IL}$	X	X	$V_{PPH}$	D <sub>IN</sub>

**NOTES:**

1. Refer to DC Characteristics.
2. X can be  $V_{IL}$ ,  $V_{IH}$  for control pins and addresses,  $V_{PPLK}$  or  $V_{PPH}$  for  $V_{PP}$ .
3. See DC Characteristics for  $V_{PPLK}$ ,  $V_{PPH}$ ,  $V_{HH}$ ,  $V_{ID}$  voltages.
4. Manufacturer and device codes may also be accessed via a CUI write sequence,  $A_1-A_{17} = X$ .
5. Refer to Table 3 for valid  $D_{IN}$  during a write operation.
6. Command writes for program or block erase are only executed when  $V_{PP} = V_{PPH}$ .
7. To write or erase the boot block, hold RP# at  $V_{HH}$ .
8. RP# must be at  $GND \pm 0.2V$  to meet the maximum deep power-down current specified.

### 3.2.2 INTELLIGENT IDENTIFIERS

The manufacturer and device codes are read via the CUI or by taking the A<sub>9</sub> pin to V<sub>DD</sub>. Writing 90H to the CUI places the device into Intelligent Identifier read mode. A read of location 00000H outputs the manufacturer's identification code, 89H. Reading location 00001H outputs the device ID, 7CH.

The 28F002BC device ID of 7CH is identical to the E28F002BX (40-lead TSOP). It differs from the PA28F200BX (44-lead PSOP), which has a device ID of 2274H. Designers using the PA28F200BX in the x8 mode who wish to migrate to the PA28F002BC need to be mindful of this device ID difference and modify software drivers as necessary.

### 3.3 Write Operations

There are two commands that alter memory array contents: Program Setup and Erase Setup/Confirm. In addition, the Erase Suspend command suspends the WSM during an erase operation and releases the CUI to accept any Read command (so long as it is to a block other than the one being erased). Finally, there is a Clear Status Register command for resetting the contents of the status register. This command should be invoked following all operations that modify the status register.

All commands written to the CUI will be interpreted, but for any write operation to be initiated, the V<sub>PP</sub> voltage must be at V<sub>HH</sub>. Depending on the application, the design may have a switchable V<sub>PP</sub> power supply or the V<sub>PP</sub> may be "hard-wired" to 12V. The 28F002BC will function normally in either case. It is highly recommended that RP# is tied to the system RESET for data protection during unstable CPU reset and also for proper CPU / flash synchronization.

Furthermore, when attempting to modify the contents of the 28F002BC's boot block area, V<sub>HH</sub> must be applied to both V<sub>PP</sub> and RP# for the operation to be valid. Whether attempting to alter the contents of the boot block or any other memory array area, if the proper voltages are not applied to the correct input signals the write operation will be aborted. Subsequently, the status register will respond with either Bit 3 (V<sub>PP</sub> low error), Bit 4 (program error) or Bit 5 (erase error) being set (refer to Table 5 for status register definitions).

### 3.3.1 COMMAND USER INTERFACE (CUI)

The Command User Interface (CUI) serves as the interface between the microprocessor and the internal chip controller. Commands are written to the CUI using standard microprocessor write timings. The available commands (summarized in Tables 3 and 4) are Read Array, Read Intelligent Identifier, Read Status Register, Clear Status Register, Program Setup, Erase Setup/Confirm, and Erase Suspend.

For Read commands, the CUI points the read path at either the array, the Intelligent Identifier, or the status register depending on the command received. For Program or Erase commands, the CUI informs the Write State Machine (WSM) that a Write or Erase has been requested. During the execution of a Program command, the WSM controls the programming sequences and the CUI responds only to status register reads. During an erase cycle, the CUI responds only to status register reads and Erase Suspend. After the WSM has completed its task, it will set the WSM Status bit (bit 7 of the status register) to a "1," which will also allow the CUI to respond to its full command set. Note that after the WSM has returned control to the CUI, the CUI will stay in the current command state until it receives another command.

**Table 3. Command Set Codes and Corresponding Device Mode**

Command Codes	Device Mode
00	Invalid/Reserved
10	Alternate Program Setup
20	Erase Setup
40	Program Setup
50	Clear Status Register
70	Read Status Register
90	Intelligent Identifier
B0	Erase Suspend
D0	Erase Resume/Erase Confirm
FF	Read Array

Table 4. Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array		Write	X	FFH			
Intelligent Identifier	1,2	Write	X	90H	Read	IA	IID
Read Status Register		Write	X	70H	Read	X	SRD
Clear Status Register		Write	X	50H			
Program Setup	3	Write	WA	40H	Write	WA	WD
Alternate Program Setup	3	Write	WA	10H	Write	WA	WD
Block Erase/Confirm		Write	BA	20H	Write	BA	D0H
Erase Suspend/Resume		Write	X	B0H	Write	X	D0H

**ADDRESS**

BA = Block Address  
 IA = Identifier Address  
 WA = Write Address  
 X = Don't Care

**DATA**

SRD = Status Register Data  
 IID = Intelligent Identifier Data  
 WD = Write Data

**NOTES:**

1. Bus operations are defined in Table 2.
2. Following the Intelligent Identifier command, two read operations access manufacturer and device codes respectively.
3. Either command 40H or 10H is valid.

**3.3.1.1 Command Function Description**

Device operations are selected by writing specific commands into the CUI. Tables 3 and 4 define the available commands. Status register (SR) bits are defined in Table 5.

**Invalid/Reserved**

These are unassigned commands and should not be used. Intel reserves the right to redefine these codes for future functions.

**Read Array (FFH)**

This single write cycle command points the read path at the array. If the host CPU performs a CE#/OE#-controlled Read immediately following a two-write sequence (i.e., a Program or Erase command) that started the WSM, then the device

will output status register contents. Writing two Read Array (FFH) commands to the CUI aborts the current operation and resets to read array mode.

Executing Read Array after the Erase Setup command (instead of giving Erase Confirm) causes the status register Erase and Program Status bits to be set. This indicates that an erase operation was initiated but not successfully confirmed (an Erase Confirm at this point would be ignored by the CUI). A subsequent Read Array command will point the data path at the array.

**Intelligent Identifier (90H)**

After this command is executed, the CUI points the output path to the intelligent identifier circuits. Only intelligent identifier values at addresses 0 and 1 can be read (only address A<sub>0</sub> is used in this mode; all other address inputs are ignored).

### Read Status Register (70H)

This is one of three commands that is executable while the WSM is operating. After this command is written, a read of the device will output the contents of the status register, regardless of the address presented to the device. The device automatically enters this mode after program or erase has completed.

### Clear Status Register (50H)

The WSM can set the Program Status and Erase Status bits in the status register to “1,” but it cannot clear them to “0.”

The status register is operated in this fashion for two reasons, the first is synchronization. Since the WSM does not know when the host CPU has read the status register, it would not know when to clear the status bits. Second, if the CPU is programming a string of bytes, it may be more efficient to query the status register after programming the string. Thus, if any errors exist while programming the string, the status register will return the accumulated error status. The Clear Status Register command clears the Program, Erase, and V<sub>PP</sub> Status bits to “0.”

### Program Setup (40H or 10H)

This command simply sets the CUI into a state such that the next write will load the Address and Data registers. After this command is executed, the outputs default to the status register. A two Read Array command sequence (FFH) is required to reset to Read Array after the Program Setup command.

### Program

The write following the Program Setup command will latch address and data. Also, the CUI initiates the WSM to begin execution of the program algorithm. The device outputs status register data when OE# is enabled. To read array data after the program operation is completed, a Read Array command is required.

### Erase Setup (20H)

The Erase Setup command prepares the CUI for the Erase Confirm command. No other action is taken. If the next command is not an Erase Confirm command, then the CUI will set both the Program Status and Erase Status bits of the status register to a “1,” place the device into Read Status Register mode, and wait for another command.

### Erase Confirm (D0H)

If the previous command was an Erase Setup command, then the CUI will enable the WSM to erase, at the same time closing the address and data latches, and respond only to the Read Status Register and Erase Suspend commands. While the WSM is executing, the device will output status register data when OE# is toggled low. Status register data can only be updated by toggling either OE# or CE#. If the previous command was not the Erase Setup command (20H), the Erase Confirm command is ignored.

### Erase Suspend (B0H)

This command is only valid while the WSM is executing an erase operation. At all other times, this command is ignored. After this command has been executed, the CUI will set a signal that directs the WSM to suspend erase operations. While waiting for the erase to be suspended, the CUI responds only to the Read Status Register command or to the Erase Resume command. Once the WSM has reached the Suspend state, it will set an output in the CUI that allows the CUI to respond to the Read Array, Read Status Register, and Erase Resume commands. In this mode, the CUI will not respond to any other commands. The WSM will also set the WSM and Erase Suspend status bits to a “1.” The WSM will continue to run, idling in the Suspend state, regardless of the state of all input control pins except V<sub>PP</sub> and RP#. If V<sub>PP</sub> is taken below V<sub>PPLK</sub>, the V<sub>PP</sub> low status bit (SR.3) will be set and the WSM will abort the suspended erase operation. If active, RP# will immediately shut down the WSM and the remainder of the chip. During a suspend operation, the data and address latches will remain closed, but the address pads are able to drive the address into the read path.

### Erase Resume (D0H)

This command will cause the CUI to clear the Suspend state and clear the WSM Status Bit to a "0," but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect under any other conditions.

### 3.3.2 STATUS REGISTER

The 28F002BC contains a status register which may be read to determine when a program or erase operation is complete, and whether that operation completed successfully. The status register may be read at any time by writing the Read Status Register command to the CUI. After writing this command, all subsequent read operations output data from the status register until another command is written to the CUI. A Read Array command must be written to the CUI to return to read array mode. The status register bits are output on DQ[0:7]. **The contents of the status register are latched on the falling edge of OE# or CE#, whichever occurs last in the read cycle.** This prevents possible bus errors that might occur if the contents of the status register change while reading the status register. CE# or OE# must be toggled with each subsequent status read to insure the status register is updated; otherwise, the completion of a program or erase operation will not be evident from the status register.

When the WSM is active, the status register will indicate the status of the WSM and upon command completion, it will indicate success or failure of the operation (see Table 5 for definition of status register bits).

#### 3.3.2.1 Clearing the Status Register

The WSM sets status bits "3" through "7" to "1," and clears bits "6" and "7" to "0," but cannot clear status bits "3" through "5" to "0." Bits 3 through 5 can only be cleared by the controlling CPU through the use of the Clear Status Register command. These bits can indicate various error conditions. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several bytes or erasing multiple blocks in sequence). The status register may then be read to determine if an error occurred during that programming or erasure series. This feature adds flexibility to the way the device may be programmed or erased. To clear the status register, the Clear Status Register command is written to the CUI. Then, any other command may be issued to the CUI. Note, again, that before a read cycle can be initiated, a valid read command must be written to the CUI to specify whether the read data is to come from the memory array, status register, or intelligent identifier.



Table 5. Status Register Bit Definition

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0
<p><b>NOTES:</b></p> <p>SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy</p> <p>SR.6 = ERASE-SUSPEND STATUS (ESS) 1 = Erase Suspended 0 = Erase In Progress/Completed</p> <p>SR.5 = ERASE STATUS 1 = Error In Block Erasure 0 = Successful Block Erase</p> <p>SR.4 = PROGRAM STATUS 1 = Error in Byte Program 0 = Successful Byte Program</p> <p>SR.3 = V<sub>PP</sub> STATUS 1 = V<sub>PP</sub> Low Detect, Operation Abort 0 = V<sub>PP</sub> OK</p> <p>SR.2–SR.0 = RESERVED FOR FUTURE ENHANCEMENTS</p>							
<p>The Write State Machine bit must first be checked to determine program or Block Erase completion, before the Program or Erase Status bits are checked for success.</p> <p>When Erase Suspend is issued, the WSM halts execution and sets both the WSMS and ESS bits to “1.” The ESS bit remains set to “1” until an Erase Resume command is issued.</p> <p>When this bit is set to “1,” the WSM has applied the maximum number of erase pulses to the block and is still unable to successfully verify block erasure.</p> <p>When this bit is set to “1,” the WSM has attempted but failed to program a byte.</p> <p>The V<sub>PP</sub> Status bit, unlike an A/D converter, does not provide continuous indication of V<sub>PP</sub> level, but it does check the V<sub>PP</sub> level intermittently. The WSM interrogates V<sub>PP</sub> level only after the program or erase command sequences have been entered, and informs the system if V<sub>PP</sub> has not been switched on. If V<sub>PP</sub> ever goes below V<sub>PPLK</sub> (even during an Erase Suspend), the status register will set this bit and abort the operation in progress, even if V<sub>PP</sub> is returned to a valid level. The V<sub>PP</sub> Status bit is not guaranteed to report accurate feedback between V<sub>PPLK</sub> and V<sub>PPH</sub>.</p> <p>These bits are reserved for future use and should be masked out when polling the status register.</p>							

### 3.3.3 PROGRAM MODE

Programming is executed using a two-write sequence. The Program Setup command is written to the CUI followed by a second write which specifies the address and data to be programmed. The WSM then executes a sequence of internally-timed events to:

1. Program the desired bits of the addressed memory byte.
2. Verify that the desired bits are sufficiently programmed.

Programming of the memory results in specific bits within a byte being changed to a “0.”

If the user attempts to program “1”s, there will be no change of in memory contents and no error is reported by the status register.

Similar to erasure, the status register indicates whether programming is complete. While the program sequence is executing, bit 7 of the status register is a “0.” The status register can be polled by toggling either CE# or OE# to determine when the program sequence is complete. Only the Read Status Register command is valid while programming is active.

When programming is complete, the status bits, which indicate whether the Program operation was successful, should be checked. If the programming operation was unsuccessful, bit 4 of the status register is set to a "1" to indicate a program failure. If bit 3 is set to a "1," then  $V_{PP}$  was not within acceptable limits, and the WSM did not execute the programming sequence. If the program operation fails, bit 4 of the status register will be set within 1.5 ms, as determined by the timeout of the WSM.

The status register should be cleared before attempting the next operation. Any CUI instruction can follow after programming is completed; however, reads from the memory array cannot be accomplished until the CUI is given the Read Array command. Figure 6 shows the Automated Programming Flowchart.

### 3.3.4 ERASE MODE

Erase Setup and Erase Confirm commands to the CUI, along with the address identifying the block to be erased. This address is latched internally when the Erase Confirm command is issued. Block erasure results in all bits within the block being set to "1."

The WSM then executes a sequence of internally timed events to:

1. Program all bits within the block to "0."
2. Verify that all bits within the block are sufficiently programmed to "0."
3. Erase all bits within the block (set all bits to "1").
4. Verify that all bits within the block are sufficiently erased.

While the erase sequence is executing, bit 7 of the status register is a "0."

When the status register indicates that erasure is complete, the status bits, which indicate whether the erase operation was successful, should be checked. If the erase operation was unsuccessful, bit 5 of the status register will be set (within 1.5 ms) to a "1," indicating an erase failure. If  $V_{PP}$  is not within acceptable during the suspended period, the WSM does not execute the erase sequence; instead, bit 5 of the status register is set to a "1" to indicate an Erase Failure, and bit 3 is set to a "1" to indicate that the  $V_{PP}$  supply voltage was outside acceptable limits.

The status register should be cleared before attempting the next operation. Any CUI instruction can follow after erasure is completed; however, reads from the memory array cannot be accomplished until the CUI is given the Read Array command. Figure 7 details the Automated Block Erase Flowchart.

#### 3.3.4.1 Suspending and Resuming Erase

Since an erase operation may take a few seconds to complete, an Erase Suspend command is provided. This allows erase-sequence interruption in order to read data from another block of the memory array. Once the erase sequence is started, writing the Erase Suspend command to the CUI requests that the WSM pause the erase sequence at a predetermined point in the erase algorithm. The status register must then be read to determine if the erase operation has been suspended. Taking  $V_{PP}$  below  $V_{PLK}$  latches the  $V_{PP}$  low status and aborts the operation in progress.  $V_{PP}$  should be maintained at valid levels, even during Erase Suspend.

At this point, a Read Array command can be written to the CUI in order to read data from blocks other than that being erased. The only other valid commands at this time are Erase Resume and Read Status Register.

During erase suspend mode, the chip can go into a pseudo-standby mode by taking  $CE\#$  to  $V_{IH}$ , which reduces active current draw.

To resume the erase operation, the chip must be enabled by taking  $CE\#$  to  $V_{IL}$ , then issuing the Erase Resume command. When the Erase Resume command is given, the WSM will continue with the erase sequence and finish erasing the block. As with the end of a standard erase operation, the status register must be read, cleared, and the next instruction issued in order to continue. Figure 8 highlights the Erase Suspend/Resume Flowchart.

### 3.3.5 EXTENDED CYCLING

Intel has designed extended cycling capability into its ETOX IV flash memory technology. The 2-Mbit Boot Block flash memory is designed for 100,000 program/erase cycles on each of the five blocks. The combination of low electric fields, clean oxide processing and minimized oxide area per memory cell subjected to the tunneling electric field results in very high cycling capability.

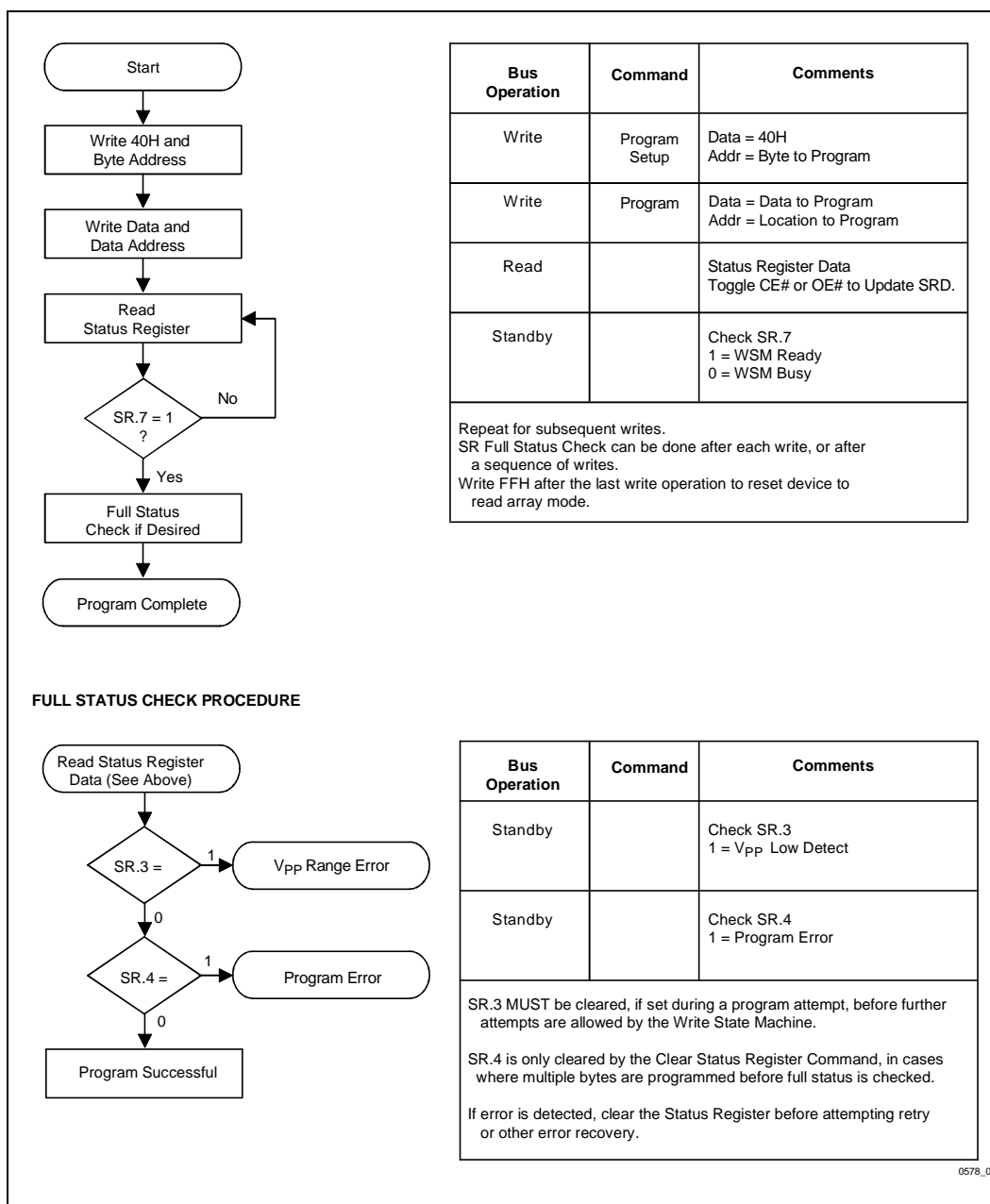
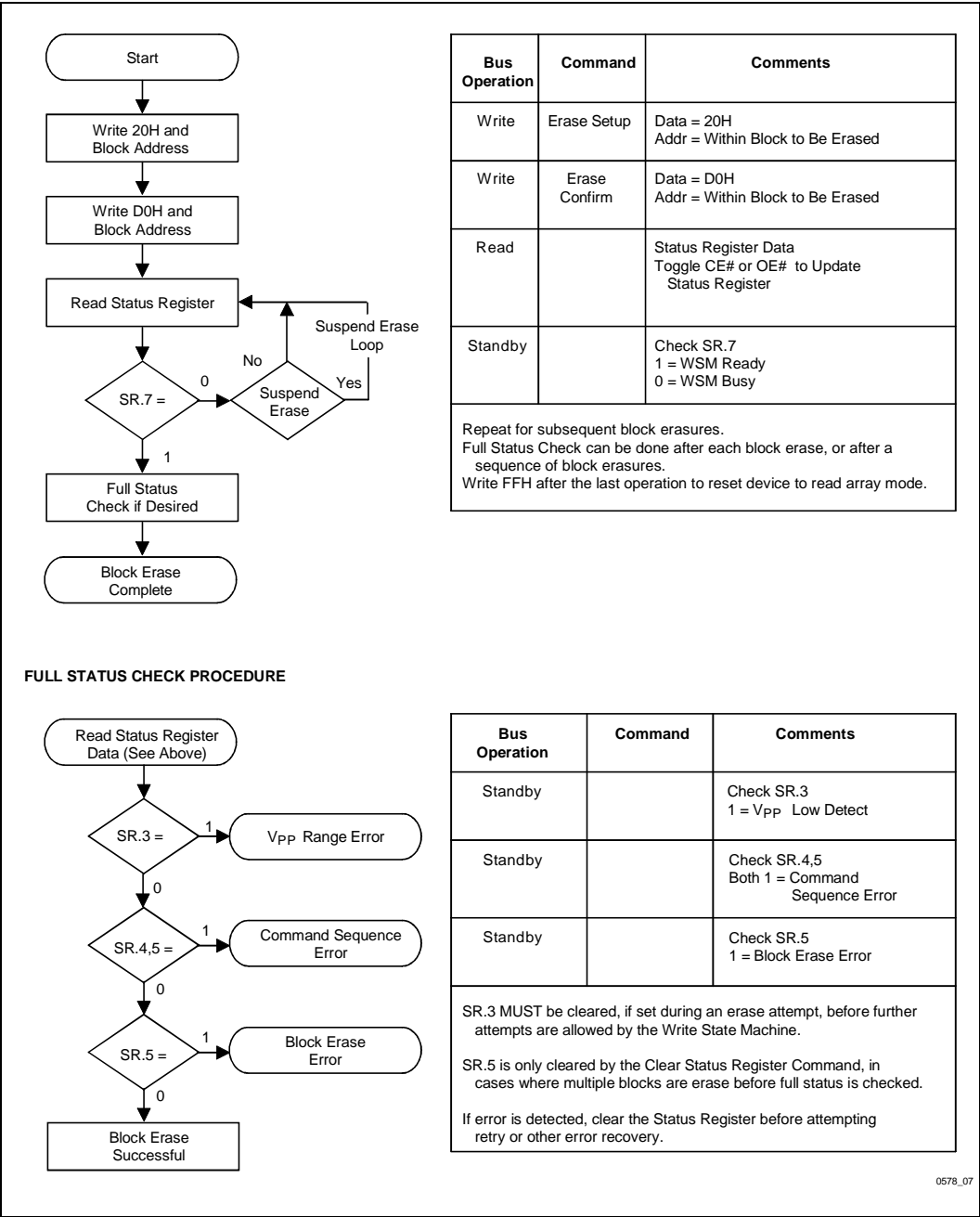


Figure 6. Automated Programming Flowchart



Read Status Register Data (See Above)

SR.3 =

V<sub>PP</sub> Range Error

SR.4,5 =

Command Sequence Error

SR.5 =

Block Erase Error

Block Erase Successful

1

0

1

0

1

0

Bus Operation	Command	Comments
Standby		Check SR.3 1 = V <sub>PP</sub> Low Detect
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error

SR.3 MUST be cleared, if set during an erase attempt, before further attempts are allowed by the Write State Machine.

SR.5 is only cleared by the Clear Status Register Command, in cases where multiple blocks are erase before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

0578\_07

Figure 7. Automated Block Erase Flowchart

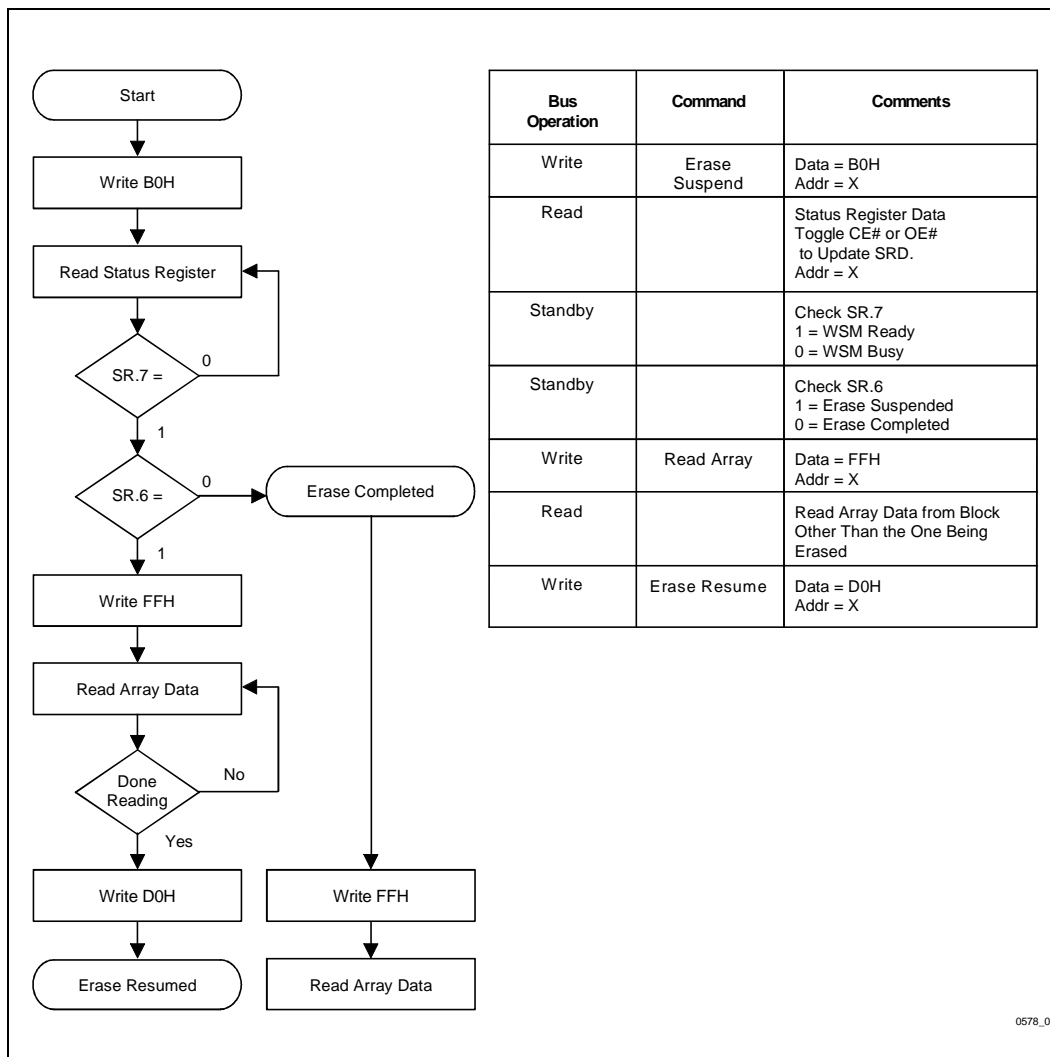


Figure 8. Erase Suspend/Resume Flowchart

### 3.4 Boot Block Locking

The Boot Block memory architecture features a hardware-lockable boot block so that the kernel code for the system can be kept secure while the parameter and main blocks are programmed and erased independently as necessary. Only the boot block can be locked independently from the other blocks.

#### 3.4.1 $V_{PP} = V_{IL}$ FOR COMPLETE PROTECTION

For complete write protection of all blocks in the flash device, the  $V_{PP}$  programming voltage can be held low. When  $V_{PP}$  is below  $V_{PPLK}$ , any program or erase operation will cause the device to set an error bit in the status register.

#### 3.4.2 $RP\# = V_{HH}$ FOR BOOT BLOCK UNLOCKING

In the case of boot block modifications (write and erase),  $RP\#$  and  $V_{PP}$  are set to  $V_{HH}$  (12V). However, if  $RP\#$  is not at  $V_{HH}$  when a program or erase operation of the boot block is attempted, the corresponding status register bit (Bit 4 for Program and Bit 5 for Erase, refer to Table 5 for status register definitions) is set to indicate the failure to complete the specified operation.

### 3.5 Power Consumption

#### 3.5.1 ACTIVE POWER

With  $CE\#$  at a logic-low level and  $RP\#$  at a logic-high level, the device is placed in the active mode. The device  $I_{CC}$  current is a maximum of 60 mA at 10 MHz with TTL input signals.

#### 3.5.2 STANDBY POWER

With  $CE\#$  at a logic-high level ( $V_{IH}$ ), the memory is placed in standby mode, where the maximum  $I_{CC}$  standby current is 100  $\mu$ A. The standby operation disables much of the device's circuitry and substantially reduces device power consumption. The outputs (DQ[0:7]) are placed in a high-impedance state independent of the status of the  $OE\#$  signal. When  $CE\#$  is at a logic-high level

during erase or program, the device will continue to perform the erase or program function and consume erase or program active power until erase or program is completed.

#### 3.5.3 DEEP POWER-DOWN

The 28F002BC flash memory supports a typical  $I_{CC}$  of 0.2  $\mu$ A in deep power-down mode. This mode is activated by the  $RP\#$  pin when it is at a logic-low ( $GND \pm 0.2V$ ); in this mode, all internal circuits are turned off to save power.

Setting the  $RP\#$  pin low de-selects the memory and places the output drivers in a high impedance state. Recovery from the deep power-down state requires a minimum access time of 300 ns (see AC Characteristics table,  $t_{PHQV}$  parameter).

During erase or program modes,  $RP\#$  low will abort either erase or program operations, but the memory contents are no longer valid as the data has been corrupted.  $RP\#$  transitions to  $V_{IL}$  or turning power off to the device will clear the status register.

### 3.6 Power-Up/Down Operation

The 28F002BC offers protection against accidental block erasure or programming during power transitions. **Power supply sequencing is not required**, since the device is indifferent as to which power supply,  $V_{PP}$  or  $V_{CC}$ , powers-up first. The CUI is reset to the read mode after power-up, but the system must drop  $CE\#$  low or present a new address to ensure valid data at the outputs.

A system designer must guard against spurious writes when  $V_{CC}$  voltages are above  $V_{LKO}$  and  $V_{PP} = V_{HH}$ . Since both  $WE\#$  and  $CE\#$  must be low for a command write, driving either signal to  $V_{IH}$  will inhibit writes to the device. The CUI architecture provides additional protection since alteration of memory contents can only occur after successful completion of the two-step command sequences. The device is also disabled until  $RP\#$  is brought to  $V_{IH}$ , regardless of the state of its control inputs. By holding the device in reset ( $RP\#$  connected to system PowerGood/Reset) during power up/down, invalid bus conditions during power-up can be masked, providing yet another level of memory protection.

### 3.6.1 RP# CONNECTED TO SYSTEM RESET

The use of RP# during system reset is important with automated write/erase devices because the system expects to read from the flash memory when it comes out of reset. If a CPU reset occurs without a flash memory reset, proper CPU initialization would not occur because the flash memory may be providing status information instead of array data. Intel's Flash memories allow proper CPU initialization following a system reset by connecting the RP# pin to the same RESET# signal that resets the system CPU.

### 3.6.2 V<sub>CC</sub>, V<sub>PP</sub> AND RP# TRANSITIONS

The CUI latches commands as issued by system software and is not altered by V<sub>PP</sub>, CE# transitions, or WSM actions. Its default state upon power-up, after exit from deep power-down mode, or after V<sub>CC</sub> transitions above V<sub>LKO</sub>, is read array mode.

After any program or block erase operation is complete, and even after V<sub>PP</sub> transitions down to V<sub>PPLK</sub>, the CUI must be reset to read array mode via the Read Array command if access to the flash memory is desired.

## 3.7 Power Supply Decoupling

Flash memory's power switching characteristics require careful device decoupling methods. System designers should consider three supply current issues:

1. Standby current levels (I<sub>CCS</sub>)
2. Active current levels (I<sub>CCR</sub>)
3. Transient peaks produced by falling and rising edges of CE#

Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each flash device should have a 0.1 μF ceramic capacitor connected between each V<sub>CC</sub> and GND, and between its V<sub>PP</sub> and GND. These high-frequency, inherently low-inductance capacitors should be placed as close as possible to the package leads.

### 3.7.1 V<sub>PP</sub> TRACE ON PRINTED CIRCUIT BOARDS

Designing for in-system writes to the flash memory requires special consideration of the V<sub>PP</sub> power supply trace by the printed circuit board designer. The V<sub>PP</sub> pin supplies the flash memory cells current for programming and erasing. One should use similar trace widths and layout considerations given to the V<sub>CC</sub> power supply trace. Adequate V<sub>PP</sub> supply traces and decoupling capacitors placed adjacent to the component will decrease spikes and overshoots.

## 4.0 ELECTRICAL SPECIFICATIONS

### 4.1 Absolute Maximum Ratings

#### Operating Temperature

During Read .....0°C to +70°C

During Write and Block Erase .....0°C to +70°C

Temperature Bias.....-10°C to +80°C

Storage Temperature .....-65°C to +125°C

Voltage on Any Pin (except  $V_{CC}$ ,  $V_{PP}$ ,  $A_9$  and  $RP\#$ )  
with Respect to GND.....-2.0V to +7.0V<sup>(1)</sup>

Voltage on Pin  $RP\#$  or Pin  $A_9$   
with Respect to GND.....-2.0V to +13.5V<sup>(1, 2)</sup>

$V_{PP}$  Program Voltage  
with Respect to GND during Write  
and Block Erase.....-2.0V to +14.0V<sup>(1, 2)</sup>

$V_{CC}$  Supply Voltage  
with Respect to GND.....-2.0V to +7.0V<sup>(1)</sup>

Output Short Circuit Current ..... 100 mA<sup>(3)</sup>

#### NOTES:

1. Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <20 ns. Maximum DC voltage on input/output pins is  $V_{CC} + 0.5V$  which, during transitions, may overshoot to  $V_{CC} + 2.0V$  for periods <20 ns.
2. Maximum DC voltage on  $V_{PP}$  may overshoot to +14.0V for periods <20 ns. Maximum DC voltage on  $RP\#$  or  $A_9$  may overshoot to 13.5V for periods <20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

NOTICE: This datasheet contains preliminary information on new products in production. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

\* **WARNING:** Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may effect device reliability.

### 4.2 Operating Conditions

Table 6. Temperature and  $V_{CC}$  Operating Conditions

Symbol	Parameter	Notes	Min	Max	Units
$T_A$	Operating Temperature		0	70	°C
$V_{CC}$	5V $V_{CC}$ Supply Voltage (10%)		4.50	5.50	Volts



4.2.1 CAPACITANCE

T<sub>A</sub> = +25° C, f = 1 MHz

Symbol	Parameter	Notes	Typ	Max	Unit	Conditions
C <sub>IN</sub>	Input Capacitance	1	6	8	pF	V <sub>IN</sub> = 0V
C <sub>OUT</sub>	Output Capacitance	1, 2	10	12	pF	V <sub>OUT</sub> = 0V

NOTES:

- 1. Sampled, not 100% tested.
- 2. For the 28F002BC, address pin A<sub>10</sub> follows the C<sub>OUT</sub> capacitance numbers.

4.2.2 INPUT/OUTPUT TEST CONDITIONS

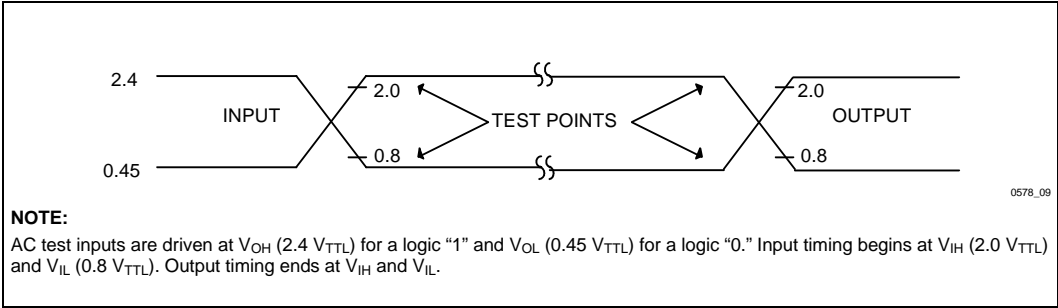


Figure 9. Inputs and Measurement Points

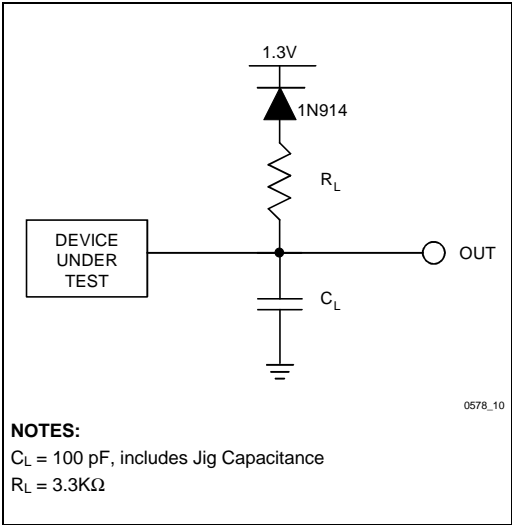


Figure 10. Standard Test Configuration

## 4.2.3 DC CHARACTERISTICS

Table 7. DC Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
$I_{IL}$	Input Load Current	1			$\pm 1.0$	$\mu A$	$V_{CC} = V_{CC} \text{ Max}$ $V_{IN} = V_{CC} \text{ or GND}$
$I_{LO}$	Output Leakage Current	1			$\pm 10$	$\mu A$	$V_{CC} = V_{CC} \text{ Max}$ $V_{IN} = V_{CC} \text{ or GND}$
$I_{CCS}$	$V_{CC}$ Standby Current	1,3			1.5	mA	$V_{CC} = V_{CC} \text{ Max}$ $CE\# = RP\# = WP\# = V_{IH}$
				50	100	$\mu A$	$V_{CC} = V_{CC} \text{ Max}$ $CE\# = RP\# = V_{CC} \pm 0.2V$
$I_{CCD}$	$V_{CC}$ Deep Power-Down Current	1		0.2	8.0	$\mu A$	$V_{CC} = V_{CC} \text{ Max}$ $V_{IN} = V_{CC} \text{ or GND}$ $RP\# = GND \pm 0.2V$
$I_{CCR}$	$V_{CC}$ Read Current	1,5		20	55	mA	<b>CMOS INPUTS</b> $V_{CC} = V_{CC} \text{ Max}$ $CE\# = GND$ $f = 10 \text{ MHz}$ $I_{OUT} = 0 \text{ mA}$ CMOS Inputs: $GND \pm 0.2V$ or $V_{CC} \pm 0.2V$
				20	60	mA	<b>TTL INPUTS</b> $V_{CC} = V_{CC} \text{ Max}$ $CE\# = V_{IL}$ $f = 10 \text{ MHz}$ $I_{OUT} = 0 \text{ mA}$ TTL Inputs: $V_{IL}$ or $V_{IH}$
$I_{CCW}$	$V_{CC}$ Write Current	1,4			50	mA	Byte Write in Progress
$I_{CCE}$	$V_{CC}$ Erase Current	1,4			30	mA	Block Erase in Progress
$I_{CCES}$	$V_{CC}$ Erase Suspend Current	1,2		5	10	mA	$CE\# = V_{IH}$ Block Erase Suspend
$I_{PPS}$	$V_{PP}$ Standby Current	1			$\pm 10$	$\mu A$	$V_{PP} \leq V_{CC}$
$I_{PPD}$	$V_{PP}$ Deep Power-Down Current	1			5.0	$\mu A$	$RP\# = GND \pm 0.2V$
$I_{PPR}$	$V_{PP}$ Read Current	1			200	$\mu A$	$V_{PP} > V_{CC}$
$I_{PPW}$	$V_{PP}$ Write Current	1,4			20	mA	$V_{PP} = V_{PPH}$ Byte Write in Progress
$I_{PPE}$	$V_{PP}$ Erase Current	1,4			15	mA	$V_{PP} = V_{PPH}$ Block Erase in Progress
$I_{PPES}$	$V_{PP}$ Erase Suspend Current	1			200	$\mu A$	$V_{PP} = V_{PPH}$ Block Erase Suspended

Table 7. DC Characteristics (Continued)

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
$I_{RP\#}$	RP# Boot Block Unlock Current	1,4			500	$\mu A$	RP# = $V_{HH}$
$I_{ID}$	A <sub>9</sub> Intelligent Identifier Current	1,4			500	$\mu A$	A <sub>9</sub> = $V_{ID}$
$V_{ID}$	A <sub>9</sub> Intelligent Identifier Voltage		10.8		13.2	V	
$V_{IL}$	Input Low Voltage		-0.5		0.8	V	
$V_{IH}$	Input High Voltage		2.0		$V_{CC} + 0.5V$	V	
$V_{OL}$	Output Low Voltage				0.45	V	$V_{CC} = V_{CC\ Min}$ $I_{OL} = 5.8\ mA$
$V_{OH}$	Output High Voltage (TTL)		2.4			V	$V_{CC} = V_{CC\ Min}$ $I_{OH} = -2.5\ mA$
	Output High Voltage (CMOS)		0.85 $V_{CC}$			V	$V_{CC} = V_{CC\ Min}$ $I_{OH} = -1.5\ mA$
			$V_{CC} - 0.4V$				$V_{CC} = V_{CC\ Min}$ $I_{OH} = -100\ \mu A$
$V_{PPLK}$	$V_{PP}$ Lock-Out Voltage	3	0.0		6.5	V	Complete Write Protection
$V_{PPH}$	$V_{PP}$ (Program/Erase Operations)	7	11.4	12.0	12.6	V	
$V_{PPH}$	$V_{PP}$ (Program/Erase Operations)	8	10.8	12.0	13.2	V	
$V_{LKO}$	$V_{CC}$ Erase/Write Lock Voltage		2.0			V	
$V_{HH}$	RP# Unlock Voltage	8	10.8	12.0	13.2	V	Boot Block Unlock Voltage

**NOTES:**

1. All currents are in RMS unless otherwise noted. Typical values at  $V_{CC} = 5.0V$ ,  $V_{PP} = 12.0V$ ,  $T = 25^{\circ}C$ . These currents are valid for all product versions (packages and speeds).
2.  $I_{CCES}$  is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of  $I_{CCES}$  and  $I_{CCR}$ .
3. Block erases and byte writes are inhibited when  $V_{PP} = V_{PPLK}$ , and not guaranteed in the range between  $V_{PPH}$  and  $V_{PPLK}$ .
4. Sampled, not 100% tested.
5. CMOS Inputs are either  $V_{CC} \pm 0.2V$  or  $GND \pm 0.2V$ . TTL Inputs are either  $V_{IL}$  or  $V_{IH}$ .
6.  $V_{CC} = 12.0V \pm 10\%$  for applications requiring 100,000 block erase cycles.
7.  $V_{PP} = 12.0V \pm 5\%$  for applications requiring 100,000 block erase cycles.
8.  $V_{PP} = 12.0V \pm 10\%$  for applications requiring wider  $V_{PP}$  tolerances at 100 block erase cycles. Note that erase times are close to maximum spec limits when using this option.

## 4.2.4 AC CHARACTERISTICS

Table 8. AC Characteristics: Read Only Operations

Symbol	Parameter	Notes	28F002BC-80		28F002BC-120		Units
			V <sub>CC</sub> = 5V ± 10% 100 pF		V <sub>CC</sub> = 5V ± 10% 100 pF		
			Min	Max	Min	Max	
t <sub>AVAV</sub>	Read Cycle Time		80		120		ns
t <sub>AVQV</sub>	Address to Output Delay			80		120	ns
t <sub>ELQV</sub>	CE# to Output Delay	2		80		120	ns
t <sub>PHQV</sub>	RP# to Output Delay			300		300	ns
t <sub>GLQV</sub>	OE# to Output Delay	2		40		40	ns
t <sub>ELQX</sub>	CE# to Output in Low Z	3	0		0		ns
t <sub>EHQZ</sub>	CE# to Output in High Z	3		30		30	ns
t <sub>GLQX</sub>	OE# to Output in Low Z	3	0		0		ns
t <sub>GHQZ</sub>	OE# to Output in High Z	3		30		30	ns
t <sub>OH</sub>	Output Hold from Address, CE#, or OE# Change, Whichever Occurs First	3	0		0		ns

## NOTES:

1. See AC Input/Output Reference Waveform for timing measurements.
2. OE# may be delayed up to  $t_{CE} - t_{OE}$  after the falling edge of CE# without impact on  $t_{CE}$ .
3. Sampled, but not 100% tested.
4. See Standard Test Configuration (Figure 10).

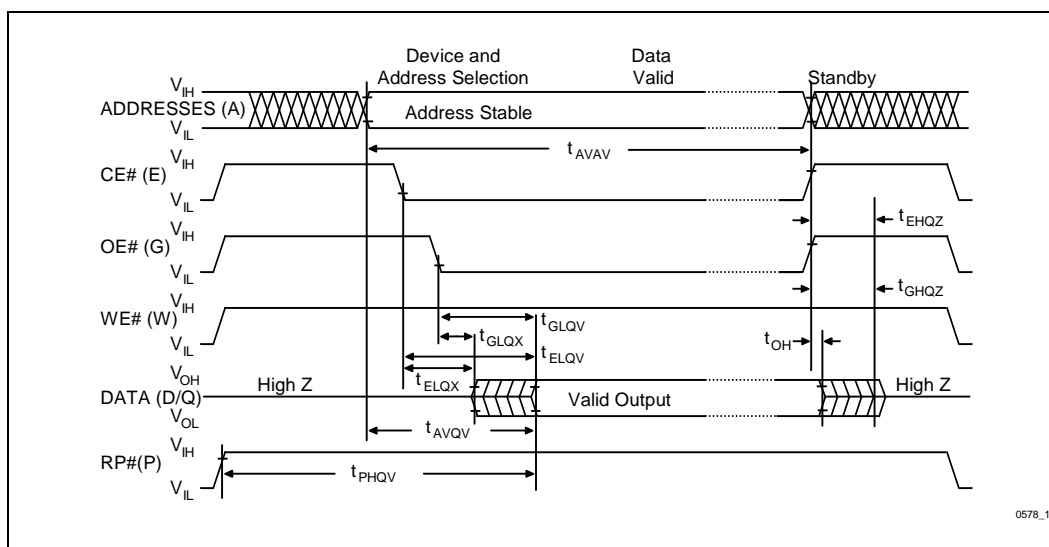


Figure 11. AC Waveforms for Read Operations

Table 9. AC Characteristics: WE#—Controlled Write Operations(1)

Symbol	Parameter	Notes	28F002BC-80		28F002BC-120		Units
			V <sub>CC</sub> = 5V ± 10% 100 pF		V <sub>CC</sub> = 5V ± 10% 100 pF		
			Min	Max	Min	Max	
t <sub>AVAV</sub>	Write Cycle Time		80		120		ns
t <sub>PHWL</sub>	RP# Setup to WE# Going Low		215		215		ns
t <sub>ELWL</sub>	CE# Setup to WE# Going Low		0		0		ns
t <sub>PHHWH</sub>	Boot Block Lock Setup to WE# Going High	6, 8	100		100		ns
t <sub>VPWH</sub>	V <sub>PP</sub> Setup to WE# Going High	5, 8	100		100		ns
t <sub>AVWH</sub>	Address Setup to WE# Going High	3	50		50		ns
t <sub>DVWH</sub>	Data Setup to WE# Going High	4	50		50		ns
t <sub>WLWH</sub>	WE# Pulse Width		50		50		ns
t <sub>WHDX</sub>	Data Hold Time from WE# High	4	0		0		ns
t <sub>WHAX</sub>	Address Hold Time from WE# High	3	0		0		ns
t <sub>WHEH</sub>	CE# Hold Time from WE# High		0		0		ns

Table 9. AC Characteristics: WE#—Controlled Write Operations(1) (Continued)

Symbol	Parameter	Notes	28F002BC-80		28F002BC-120		Units
			V <sub>CC</sub> = 5V ± 10% 100 pF		V <sub>CC</sub> = 5V ± 10% 100 pF		
			Min	Max	Min	Max	
t <sub>WHWL</sub>	WE# Pulse Width High		20		20		ns
t <sub>WHQV1</sub>	Duration of Programming Operation	2, 5	6		6		μs
t <sub>WHQV2</sub>	Duration of Erase Operation (Boot)	2, 5, 6	0.3		0.3		s
t <sub>WHQV3</sub>	Duration of Erase Operation (Parameter)	2,5	0.3		0.3		s
t <sub>WHQV4</sub>	Duration of Erase Operation (Main)	2, 5	0.6		0.6		s
t <sub>QVVL</sub>	V <sub>PP</sub> Hold from Valid SRD	5, 8	0		0		ns
t <sub>QVPH</sub>	RP# V <sub>HH</sub> Hold from Valid SRD	6, 8	0		0		ns
t <sub>PHBR</sub>	Boot-Block Relock Delay	7, 8		100		100	ns

**NOTES:**

1. Read timing characteristics during write and erase operations are the same as during read-only operations. Refer to AC characteristics during read mode.
2. The on-chip WSM completely automates program/erase operations; program/erase algorithms are now controlled internally which includes verify and margining operations.
3. Refer to command definition table for valid  $A_{IN}$ .
4. Refer to command definition table for valid  $D_{IN}$ .
5. Program/erase durations are measured to valid SRD data (successful operation, SR.7 = 1).
6. For boot block program/erase, RP# should be held at  $V_{HH}$  until operation completes successfully.
7. Time  $t_{PHBR}$  is required for successful relocking of the boot block.
8. Sampled, but not 100% tested.

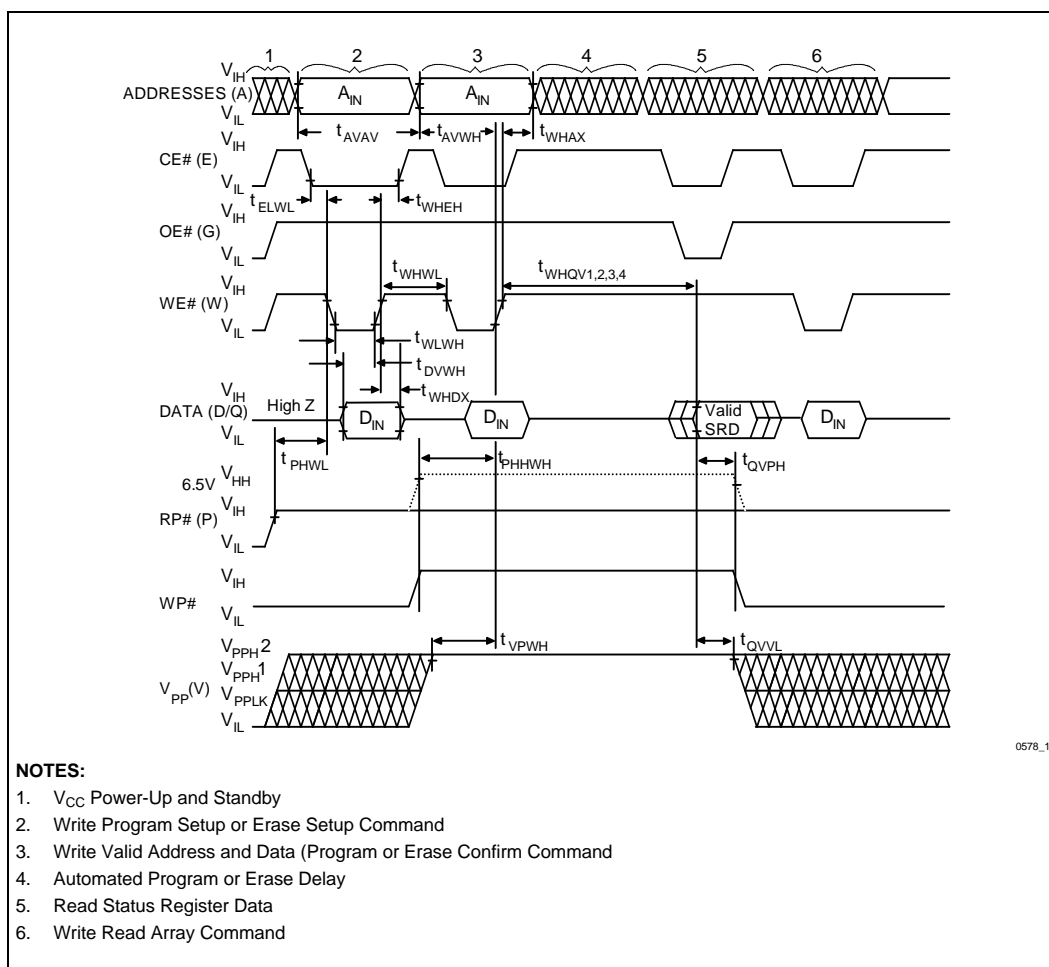


Figure 12. AC Waveforms for Write and Erase Operations (WE#—Controlled Writes)

Table 10. AC Characteristics: CE#—Controlled Write Operations<sup>(1,9)</sup>

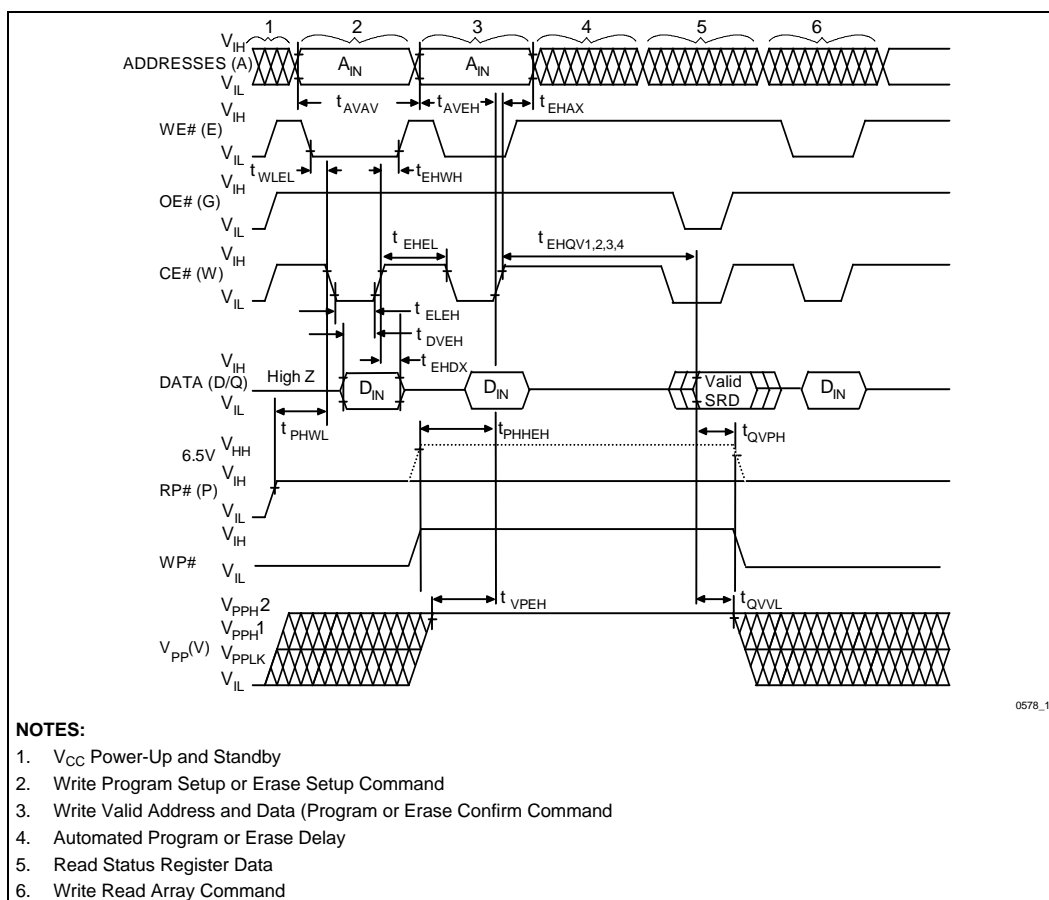
Symbol	Parameter	Notes	28F002BC-80		28F002BC-120		Units
			V <sub>CC</sub> = 5V ± 10% 100 pF		V <sub>CC</sub> = 5V ± 10% 100 pF		
			Min	Max	Min	Max	
t <sub>AVAV</sub>	Write Cycle Time		80		120		ns
t <sub>PHEL</sub>	RP# High Recovery to CE# Going Low		215		215		ns
t <sub>WLEL</sub>	WE# Setup to CE# Going Low		0		0		ns
t <sub>PHHEH</sub>	Boot Block Lock Setup to CE# Going High	6, 8	100		100		ns
t <sub>VPEH</sub>	V <sub>PP</sub> Setup to CE# Going High	5, 8	100		100		ns
t <sub>AVEH</sub>	Address Setup to CE# Going High	3	50		50		ns
t <sub>DVEH</sub>	Data Setup to CE# Going High	4	50		50		ns
t <sub>ELEH</sub>	CE# Pulse Width		50		50		ns
t <sub>EHDx</sub>	Data Hold Time from CE# High	4	0		0		ns
t <sub>EHAX</sub>	Address Hold Time from CE# High	3	0		0		ns
t <sub>EHWL</sub>	WE # Hold Time from CE# High		0		0		ns
t <sub>EHEL</sub>	CE# Pulse Width High		30		30		ns
t <sub>EHQV1</sub>	Duration of Programming Operation	2, 5	6		6		μs
t <sub>EHQV2</sub>	Duration of Erase Operation (Boot)	2, 5, 6	0.3		0.3		s
t <sub>EHQV3</sub>	Duration of Erase Operation (Parameter)	2, 5	0.3		0.3		s
t <sub>EHQV4</sub>	Duration of Erase Operation (Main)	2, 5	0.6		0.6		s
t <sub>QVVL</sub>	V <sub>PP</sub> Hold from Valid SRD	5, 8	0		0		ns
t <sub>QVPH</sub>	RP# V <sub>HH</sub> Hold from Valid SRD	6, 8	0		0		ns
t <sub>PHBR</sub>	Boot Block Relock Delay	7, 8		100		100	ns

**NOTES:**

See WE# Controlled Write Operations for notes 1 through 8.

9. Chip-Enable controlled writes: write operations are driven by the valid combination of CE# and WE# in systems where CE# defines the write pulse-width (within a longer WE# timing waveform), all set-up, hold and inactive WE# times should be measured relative to the CE# waveform.





**Figure 13. Alternate AC Waveforms for Write and Erase Operations (CE#—Controlled Writes)**

**Table 11. Erase and Program Timings ( $T_A = +25^\circ\text{C}$ )**

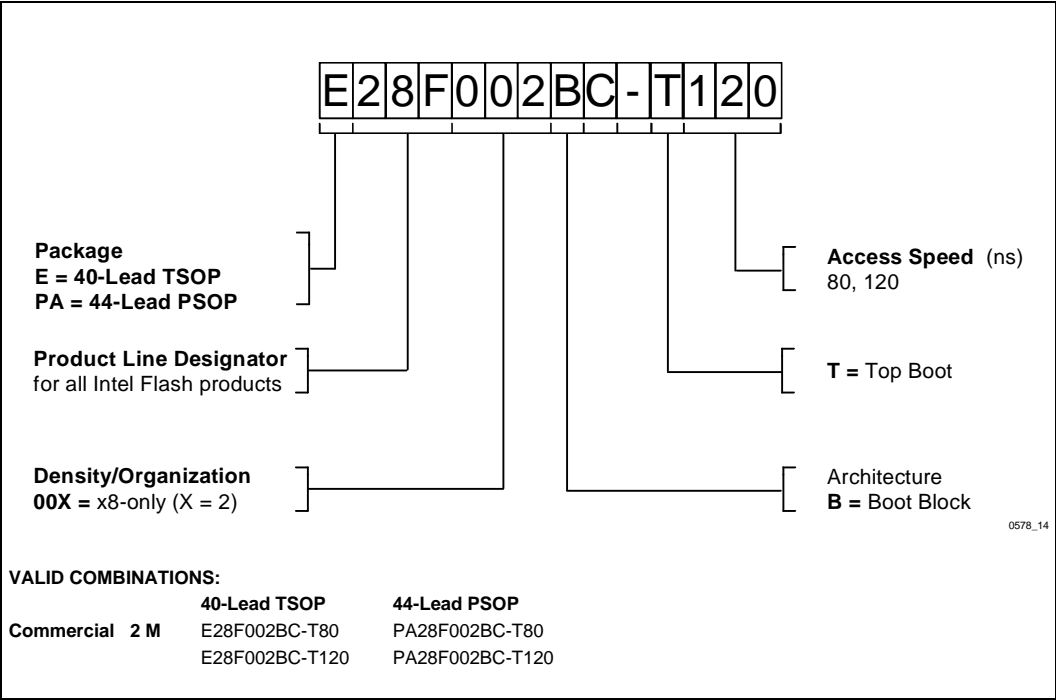
Parameter <sup>1</sup>	V <sub>PP</sub> = 12V ± 10% <sup>2</sup>		V <sub>PP</sub> = 12V ± 5%		Units
	V <sub>CC</sub> = 5V ± 10%		V <sub>CC</sub> = 5V ± 10%		
	Typ	Max	Typ	Max	
Boot/Parameter Block Erase Time	5.8	40	1.0	7	s
Main Block Erase Time	14	60	2.4	14	s
Main Block Write Time	6.0	20	1.2	4.2	s

**NOTES:**

1. All numbers are sampled, not 100% tested.
2. Erase times near max limits when the 10%  $V_{PP}$  option is used.



APPENDIX A  
ORDERING INFORMATION



## APPENDIX B ADDITIONAL INFORMATION

### RELATED INTEL INFORMATION<sup>(1,2)</sup>

Order Number	Document
292130	<i>AB-57 Boot Block Architecture for Safe Firmware Updates</i>
292098	<i>AP-363 Extended Flash BIOS Concepts for Portable Computers</i>
292148	<i>AP-604 Using Intel's Boot Block Flash Memory Parameter Blocks to Replace EEPROM</i>
292161	<i>AP-608 Implementing a Plug and Play BIOS Using Intel's Boot Block Flash Memory</i>
292163	<i>AP-610 Flash Memory In-System Code and Data Update Techniques</i>
290448	<i>28F002/200BX-T/B 2-Mbit Boot Block Flash Memory Datasheet</i>
290451	<i>28F004/400BX-T/B 4-Mbit Boot Block Flash Memory Datasheet</i>
290531	<i>28F002/200BV-T/B 2-Mbit SmartVoltage Flash Memory Datasheet</i>
290530	<i>28F004/400BV-T/B 4-Mbit SmartVoltage Flash Memory Datasheet</i>

#### NOTES:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at <http://www.Intel.com> for technical documentation and tools.